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FIG. 1

Inventors: HONGZHOU LIU et al.
"METHOD AND APPARATUS FOR QUANTIFYING TRADEOFFS FOR MULTIPLE COMPETING
GOALS IN CIRCUIT DESIGN"
Attorney Docket No.: 2879-030565   Application No. 10/652,018

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FIG. 2

DEVICE(S)			SYNTHESIZED PERFORMANCE ✱ SPECIFICATION(S)
DEVICE #	DEVICE VARIABLE(S)	DEVICE CONSTANTS(S)	
D1 (INPUT TRANSISTOR)	LENGTH & WIDTH	AREA	GAIN (G)
D2 (INPUT TRANSISTOR)	=	=	SLEW RATE (SR)
D3 (INPUT TRANSISTOR)	=	=	UNITY GAIN FREQ (UGF)
D4 (RESISTOR)	RESISTANCE	LENGTH & WIDTH	INPUT OFFSET (IO)
D5 (CAPACITOR)	CAPACITANCE	=	PHASE MARGIN (PM)
D6 (RESISTOR)		=	
D7 (CAPACITOR)		=	
D8 (RESISTOR)	RESISTANCE		

TO FROM A-A

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FIG. 2

TO FROM A-A

			SETTLING TIME (ST)
D9 (RESISTOR)	=		POWER (USAGE) (P)
D10 (RESISTOR)	=		
D11 (OUTPUT TRANSISTOR)	LENGTH & WIDTH	AREA	ESTIMATED TOTAL AREA (ETA)
D12 (OUTPUT TRANSISTOR)	=	AREA	

* PERFORMANCE SPECIFICATIONS TO BE COMPARED
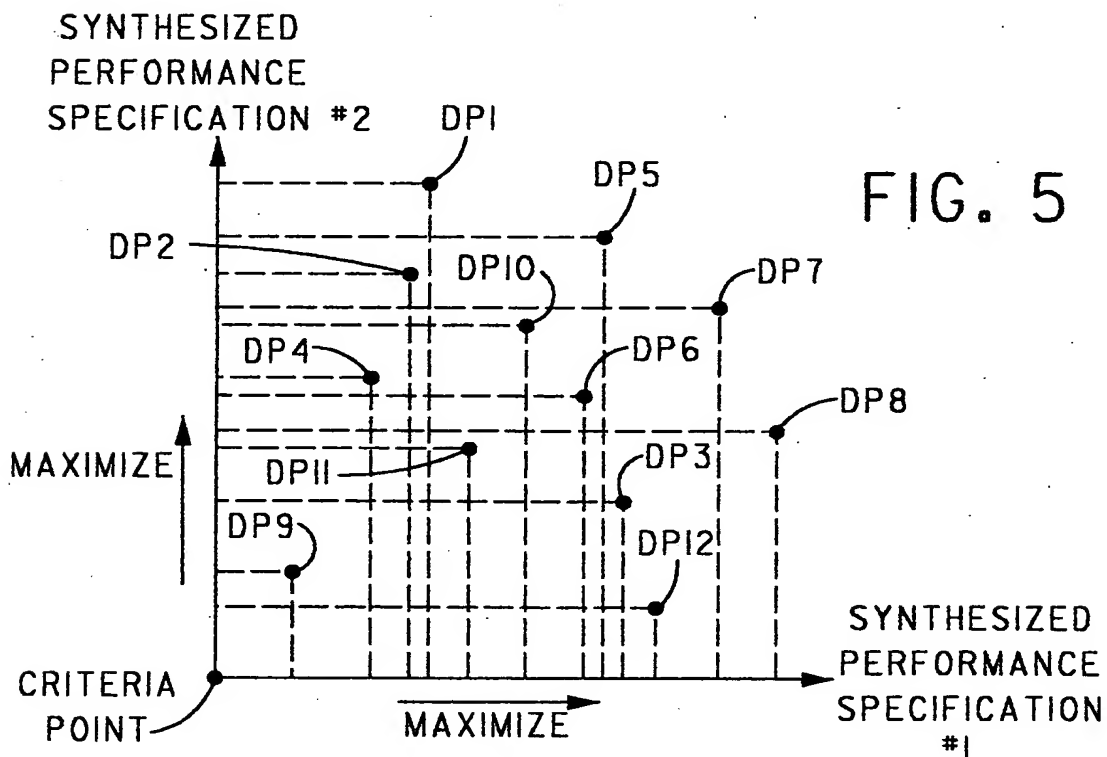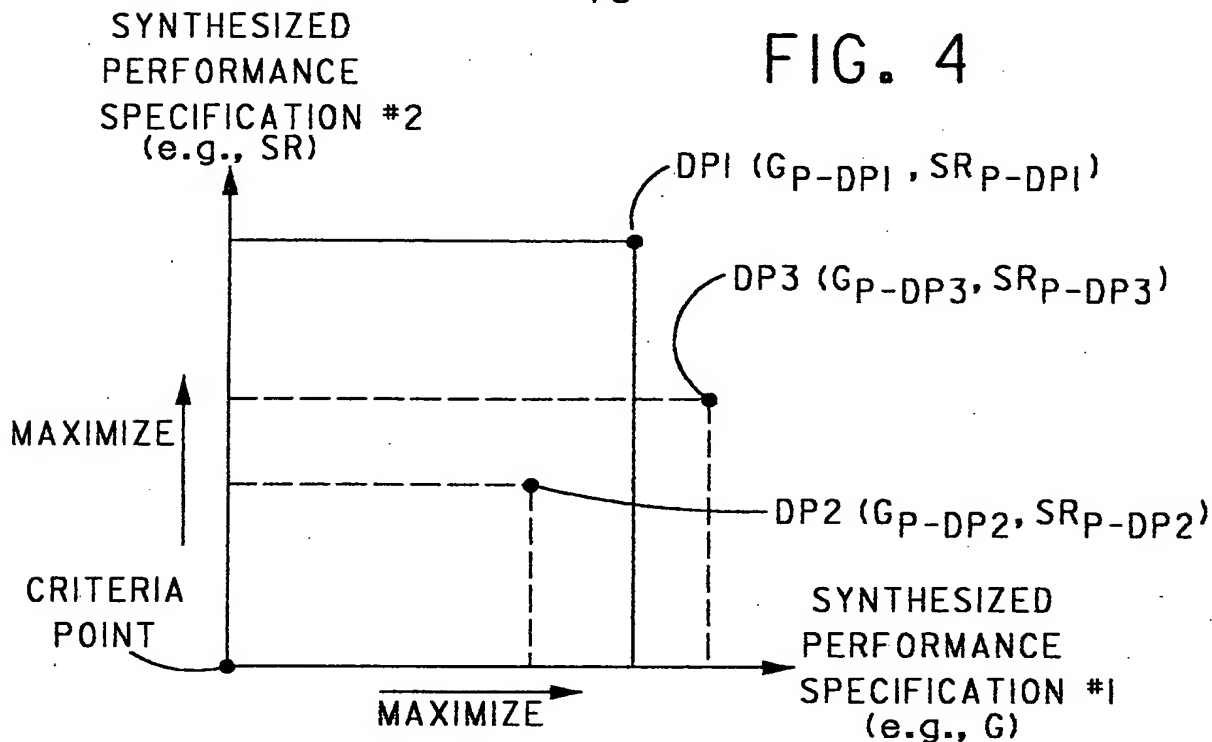TO CIRCUIT PERFORMANCES DETERMINED BY A
CIRCUIT SYNTHESIZER

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FIG. 3

SYNTHESIZED
DESIGN POPULATION

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DESIGN POINT	CIRCUIT TOPOLOGY	PERFORMANCE(S)	ORIGINAL COST	DOMINATION COST	TRADEOFF COST	RELATIVE EFFICIENCY
DPI	T_{DPI}	G_{P-DPI} SR_{P-DPI} $\cdots$ ETA_{P-DPI}	OC_{DPI}	DC_{DPI}	TC_{DPI}	RE_{DPI}
DP5	T_{DP5}	G_{P-DP5} SR_{P-DP5} $\cdots$ ETA_{P-DP5}	OC_{DP5}	DC_{DP5}	TC_{DP5}	RE_{DP5}
DP7	T_{DP7}	G_{P-DP7} SR_{P-DP7} $\cdots$ ETA_{P-DP7}	OC_{DP7}	DC_{DP7}	TC_{DP7}	RE_{DP7}
$\cdots$			$\cdots$		$\cdots$	$\cdots$
DPX	T_{DPX}	G_{P-DPX} SR_{P-DPX} $\cdots$ ETA_{P-DPX}	OC_{DPX}	DC_{DPX}	TC_{DPX}	RE_{DPX}

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FIG. 4

FIG. 5

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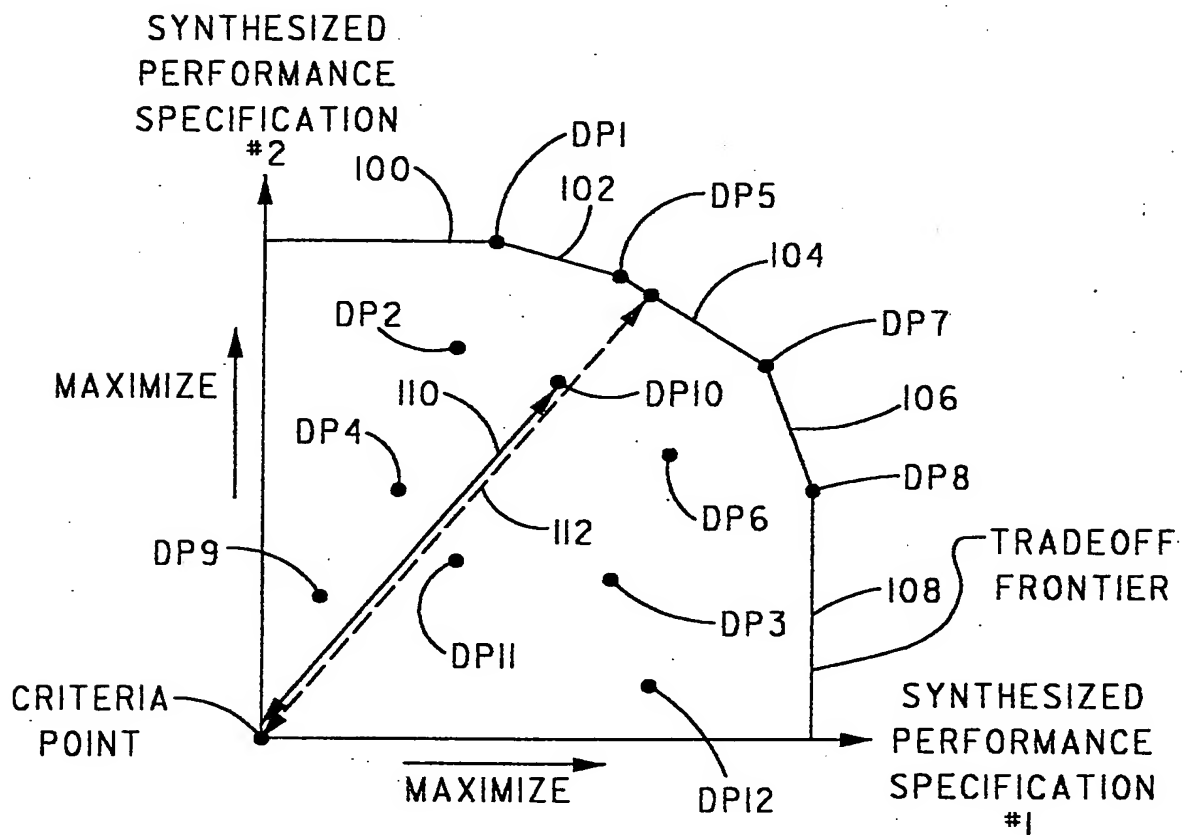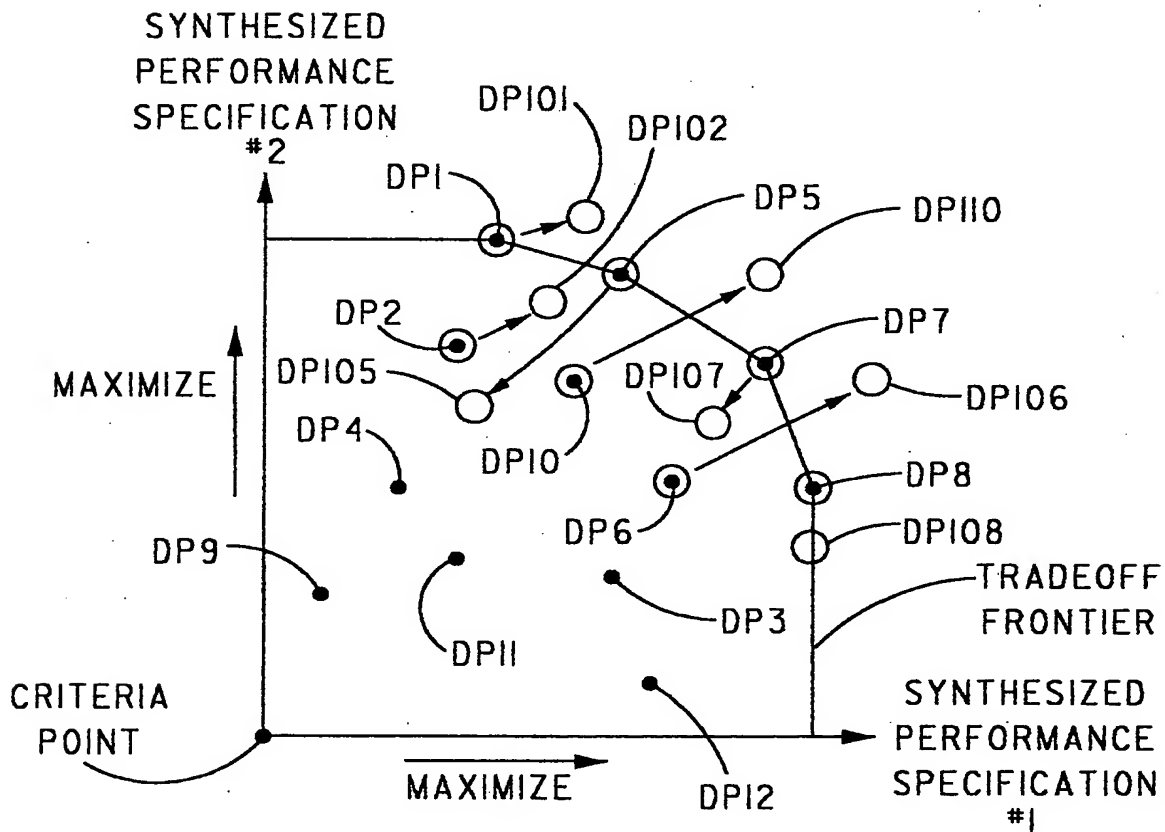

FIG. 6

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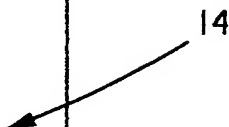⊙ = DESIGN POINTS WITH LOWEST
     TRADEOFF COST

○ = NEW DESIGN POINTS GENERATED FROM
     DESIGN POINTS WITH LOWEST
     TRADEOFF COSTS

FIG. 7

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                LAYOUT
             PERFORMANCE
           SPECIFICATIONS *
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GAIN (G)

SLEW RATE (SR)

UNITY GAIN FREQ. (UGF)

INPUT OFFSET (IO)

PHASE MARGIN (PM)

SETTLING TIME (ST)

POWER (USEAGE) (P)

ACTUAL TOTAL AREA (ATA)

YIELD ESTIMATE (YE)

DESIGN RULE COMPLIANCE (DRC)

* PERFORMANCE SPECIFICATIONS TO BE COMPARED
 TO CIRCUIT PERFORMANCES DETERMINED BY A
  CIRCUIT SIMULATOR.

FIG. 8

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FIG. 9

LAYOUT DESIGN POPULATION

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LAYOUT DESIGN POINT	CIRCUIT LAYOUT	PERFORMANCE(S)	ORIGINAL COST	DOMINATION COST	TRADEOFF COST	RELATIVE EFFICIENCY
LDP1	L_{LDP1}	G_{P-LDP1} SR_{P-LDP1} $\cdots$ DRC_{P-LDP1}	OC_{LDP1}	DC_{LDP1}	TC_{LDP1}	RE_{LDP1}
LDP5	L_{LDP5}	G_{P-LDP5} SR_{P-LDP5} $\cdots$ DRC_{P-LDP5}	OC_{LDP5}	DC_{LDP5}	TC_{LDP5}	RE_{LDP5}
LDP7	L_{LDP7}	G_{P-LDP7} SR_{P-LDP7} $\cdots$ DRC_{P-LDP7}	OC_{LDP7}	DC_{LDP7}	TC_{LDP7}	RE_{LDP7}
$\cdots$			$\cdots$			$\cdots$
LDPX	L_{LDPX}	G_{P-LDPX} SR_{P-LDPX} $\cdots$ DRC_{P-LDPX}	OC_{LDPX}	DC_{LDPX}	TC_{LDPX}	RE_{LDPX}

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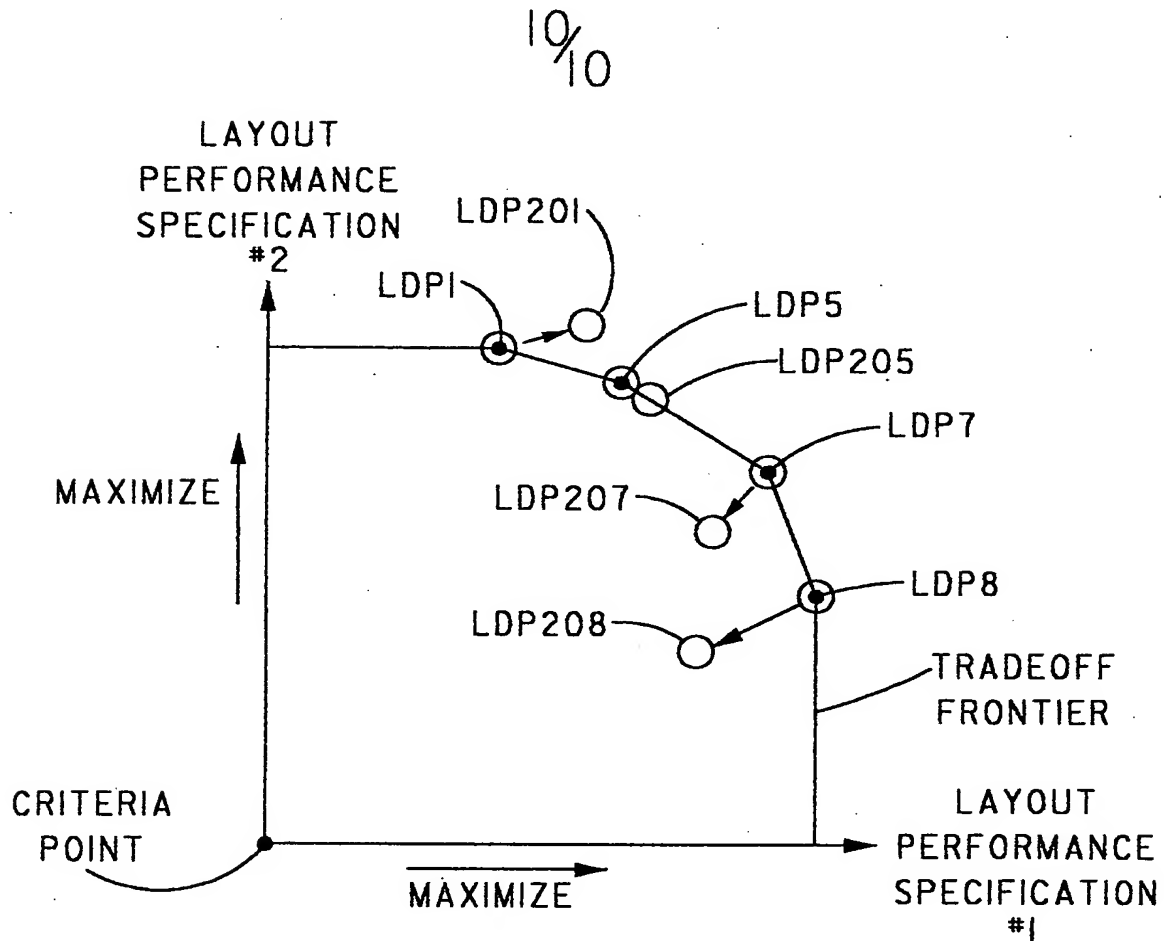
⊙ = LAYOUT DESIGN POINT GENERATED
    FROM DESIGN POINTS WITH LOWEST
    TRADEOFF COST

○ = NEW LAYOUT DESIGN POINT GENERATED
    FROM LAYOUT DESIGN POINTS GENERATED
    FROM DESIGN POINTS WITH LOWEST
    TRADEOFF COSTS

FIG. 10